(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0306 Roll No. | | | | | | | | | | |

B. Tech.

(SEM. VII) ODD SEMESTER THEORY EXAMINATION 2010-11

DIGITAL SYSTEM DESIGN USING VHDL

Time : 3 Hours *Total Marks : 100*

Note :— (1) Attempt **all** questions.

(2) All questions carry equal marks.

1. Answer any **four** parts of the following : **(5×4=20)**

   (a) Write VHDL description of an SR latch.

   (b) Write the VHDL code for a full subtracter using logic equation.

   (c) Write short notes on (a) VHDL Function (b) VHDL Procedures.

   (d) Discuss the predefined VHDL operators.

   (e) Write a VHDL model for the 74163 counter.

   (f) Using waveforms explain the VHDL delays.

2. Answer any **two** parts of the following : **(10×2=20)**

   (a) Enlist the IEEE standard specified a logic value for use with VHDL. Write the VHDL code for 4 × 1 MUX.

   (b) Draw a Block diagram for binary multiplier. Write a behavioural model for 4 × 4 Binary multiplier, maximum number of clock cycle needed for a multiply is 10.

(c) Explain the following term (i) GENERICS (ii) SYNTHESIS of VHDL code (iii) FILES and TEXTIO.

3. Answer any **two** parts of the following : **(10×2=20)**

(a) Draw a block diagram for Dice Game. Discuss the SM chart and behavioural model for Dice Game.

(b) What are the various floating point operations ? Draw and explain the flow chart for floating point multiplication.

(c) Explain the model for 2's complement multiplier (4-bit multiplier for 2's complement numbers and implements the controller using a counter and logic equations).

4. Answer any **two** parts of the following : **(10×2=20)**

(a) Using block diagram of RAM system explain the SM chart of RAM system.

(b) Draw and explain SM chart for simplified 486 bus interface.

(c) Explain the UART block diagram with SM chart for the Transmitter.

5. Answer any **two** parts of the following : **(10×2=20)**

(a) Write a VHDL code for simple 6116 state RAM model.

(b) Draw a block diagram for M68HC05 Microcontroller. Write various addressing modes of 6805 microcontroller.

(c) Write short notes on the following (a) Xilinx 3000 series FPGAs (b) VHDL code for memory controller.