Printed pages: 01 **Sub Code: NEC703**

Paper Id: | 3 | 0 | 5 | 7 | **Roll No:** | | | | | | | | | | |

B.TECH

(SEM VII) THEORY EXAMINATION 2017-18

VLSI DESIGN

Time: 3 Hours ***Total Marks: 100***

Notes: *Attempt all Sections. Assume any missing data.*

SECTION A

1. Attempt any ten questions. All question carry equal marks. 10*2= 20

(a). Give the circuit arrangement for 2 input NAND gate using CMOS logic.

(b). Enlist the advantages of using address multiplexing scheme in DRAM cell.

(c). What is parasitic delay?

(d). What is the classification of IC packages?

(e). Write down the Applications of FPGA.

(f). What is sub threshold leakage current?

(g). What is crosstalk delay in VLSI?

(h). What is body effect?

(i). Implement 2:1 MUX using CMOS Transmission Gate.

(j). Write the Expression of dynamic power dissipation for MOS circuit.

SECTION B

2. **Attempt any three questions. All question carry equal marks. 3*10=30**

(a). What are various processes of CMOS fabrication? Explain Twin tub processes with suitable sketch

(b). What is need of VLSI Testing? Discuss about Functional and manufacturing tests.

(c). Derive the equation for calculation of delay in multistage logic Network in terms of path effort and parasitic delay. What are the criteria for choosing best number of stages in it?

(d). Why transistor scaling is of great importance in VLSI? Write down comparison between Constant field scaling and Constant voltage scaling.

(e). Explain CMOS Domino circuit along with its features. How it can be cascaded in VLSI circuits.

SECTION C

3. **Attempt any one part of question. All question carry equal marks. 1*10=10**

(a) What are the sources of power dissipation in CMOS circuits? Explain Dynamic and static power consumption.

(b) What are interconnecting models? Explain any two of them in brief.

4 Attempt any one question. All questions carry equal marks 1*10=10

(a) Draw the circuit diagram of SRAM and explain read and write operation.

(b) Explain the variable threshold CMOS circuits

5 Attempt any one part of question. All questions carry equal marks 1*10=10

(a) Explain the following:

(i) Ad Hoc testable design techniques. (ii) Fault types and models.

(b) Explain the concept of Design Hierarchy with the help of example.

6 **Attempt any one part of question. All questions carry equal marks 1*10=10**

(a) What are the different scan based techniques explain built in self-test technique.

(b) Explain the concept of observablity controlabllity and predictability.

7 **Attempt any one question. All questions carry equal marks 1*10=10**

(a) Explain CMOS Lambda based design rules with help of one example.

(b) Implement the CMOS logic for the following Boolean expression:

(i) Y= (A+B+C).D

(ii) Y= (A+B+C)(D+E).F

(iii) 3 input NOR gate