(b) Explain the mode 1 operation of 8253 with the help of timing waveform. What will happen if a new count is written while counter is running ?

(c) Interface a 4 ×4 matrix keyboard to 8085. Show the interfacing diagram and write a routine to read 10 key strokes and store them into memory.

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 2119 **Roll No.**

B.Tech.

(SEM. V) THEORY EXAMINATION 2011–12

MICRO-PROCESSORS

Time : 2 Hours *Total Marks : 50*

Note :– (1) Attempt all questions.

(2) Assume necessary data if required.

1. Attempt any **two** parts : **(5×2=10)**

(a) Explain the function of ***HOLD, READY, ALE*** and ***CLK OUT*** signals of 8085.

(b) Explain the function of Stack Pointer, Accumulator and HL Register Pair of 8085.

(c) Interface 16KB EPROM and 48 KB SRAM to 8085 with the help of 8KB EPROM ICs and 8KB SRAM ICs. Draw the address map and show the address decoding logic.

2. Attempt any **two** parts : **(5×2=10)**

(a) In a certain microprocessor based system 8085 has to be used to utilize its maximum hardware and software capabilities. What IO addressing scheme would you suggest for 8085 ? Justify your answer.

(b) (i) Draw a flow chart to determine maximum of three numbers.

(ii) In 8085 microprocessor what will be the status of address bus (A0-A15), read signal, write signal and $IO/\bar{M}$ during the execution of instruction **IN 45H.**

(iii) Explain, why a Latch is used as an output port.

(c) (i) After a certain ALU operation the content of accumulator is 32H and known flags are CY-1 & AC-1. Based upon this information obtain the BCD number that would be present in accumulator after the decimal adjust accumulator operation.

(ii) Explain the direct addressing mode with the help of examples.

3. Attempt any **two** parts : **(5×2=10)**

(a) Explain the operation performed by following 8085 instructions. Also name the machine cycles, in sequence, it would take for the execution

(i) XTHL

(ii) CPE 5000H

(iii) RNZ

(b) (i) What is meant by the vectored and non vectored interrupts ? List out all the vectored interrupts of 8085 and give their vector addresses.

(ii) If 8085 is currently executing an interrupt service routine and another interrupt comes then, on what conditions this new interrupt will be served ?

(iii) Write instructions to enable all vectored interrupts of 8085.

(c) Draw the machine cycle diagram for the execution of SUB C and explain the various activities shown by this diagram.

4. Attempt any **two** parts : **(5×2=10)**

(a) Write an assembly language program to generate a delay of 1 msec. Also show the calculation of time. Assume that the crystal frequency of 8085 is 6 MHz.

(b) A series of 8-bit numbers is stored in the memory. Write an 8085 assembly language program to add all the numbers in this series. The result may be 16-bit.

(c) Write an 8085 assembly language program to transfer an 8-bit data serially, through ***SOD*** line.

5. Attempt any **two** parts : **(5×2=10)**

(a) For 8086 microprocessor

(i) Explain how BIU will read from memory if the program is stored at

(1) ODD address

(2) Even address.

(ii) List out the conditions in which internal queue will be flushed out.