(ii) For the Schmitt trigger shown in fig. calculate the trip points and hysteresis is $V_{sat} = \pm 13.5$ V. If the resistance have a tolerance of ±5%, what is the minimum hysteresis ?

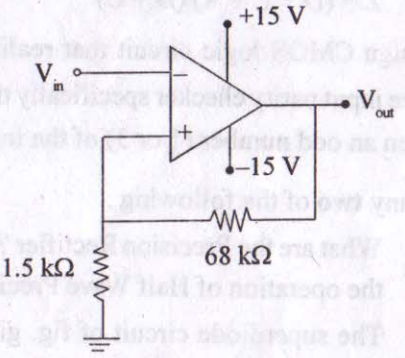

Fig. 3

(c) Write short notes on any **two** of the following :

(i) Analog Multiplier

(ii) Log and Antilog amplifier

(iii) Zero crossing detection.

5. Answer any **two** of the following : **(2×10=20)**

(a) (i) Explain working of weighted resistor D/A converter.

(ii) Determine the output voltage produced by a 4 bit DAC whose output voltage is 0 to 10 V when the input binary number is 0110.

(b) (i) Draw the circuit diagram for monostable multivibrator with operational amplifier. Explain its operation. Derive the expression for its time period.

(ii) The timer IC 555 is used as astable multivibrator. It is desired to have square wave output with 50% duty cycle of 1 kHz. The timing capacitor is of 0.01 μF. Find the values of resistors required and draw the circuit.

(c) (i) What is the principle of PLL ? Explain Lock range and Capture range with block diagram.

(ii) Describe PLL application as frequency translator.

Printed Pages—4 **EEC501**

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 2117 **Roll No.**

B. Tech.

(SEM. V) ODD SEMESTER THEORY EXAMINATION 2013-14

INTEGRATED CIRCUITS

Time : 3 Hours *Total Marks : 100*

Note : Attempt **all** questions.

1. Answer any **four** of the following : **(5×4=20)**

(a) Discuss the operation and significance of a multiple output transistor mirror.

(b) Explain Widlar current source. Fig. given below shows two circuit for generating a constant current $I_o = 10$ μA which operate from a 10 V supply. Determine the values of the required resistor assuming that V_{BE} is 0.7 V at a current of 1 mA and neglecting of the effect of finite β.

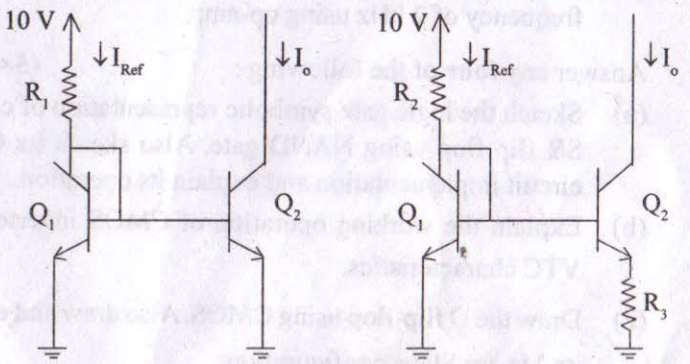

Fig. 1

(c) How the short circuit protection is achieved in the output stage of 741 op-amp ? Also, find the output resistance of 741 op-amp.

(d) A 741 IC op-amp whose slew rate is 0.5 V/μs is used as an inverting amplifier with a gain of 50. The voltage gain V_s frequency curve of 741 IC is flat upto 20 kHz. What maximum peak to peak input signal can be applied without distorting the output ?

(e) Define following parameter as applied to an amp :

(i) Input bias current

(ii) Input offset current and voltage

(iii) C.M.R.R.

(iv) P.S.R.R.

(v) Slew Rate.

2. Answer any **two** of the following : **(2×10=20)**

(a) (i) Draw and explain I-V converter and derive its output equation.

(ii) Draw V-I converter and derive its output equation for floating load.

(b) Classify active filter and write its advantages with suitable examples.

(c) Design a second order low pass filter at a high cut off frequency of 2 kHz using op-amp.

3. Answer any **four** of the following : **(5×4=20)**

(a) Sketch the logic gate symbolic representation of clocked SR flip flop using NAND gate. Also sketch its CMOS circuit implementation and explain its operation.

(b) Explain the working operation of CMOS inverter with VTC characteristics.

(c) Draw the D flip-flop using CMOS. Also draw and explain its Master Slave configuration.

(d) Sketch the CMOS logic circuit realization of the following expression :

(i) $Z = \overline{A(D + E) + BC}$

(ii) $Z = \overline{(D + E + A)(B + C)}$

(e) Design CMOS logic circuit that realize the function of three input parity checker specifically the output is to high when an odd number (1 or 3) of the input is high.

4. Answer any **two** of the following : **(2×10=20)**

(a) (i) What are the Precision Rectifier ? Draw and explain the operation of Half Wave Precision Rectifier.

(ii) The superdiode circuit of fig. given below can be made to have gain by connecting a resistor R_2 in place of the short circuit between the cathode of the diode and –ve input terminal of the op-amp, and a resistor R_1 between the –ve input terminal and ground. Design a circuit for a gain of 2. For a 10 V peak to peak input sine wave, what is the average output voltage resulting ?

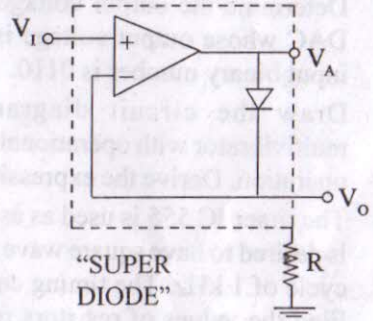

Fig. 2

(b) (i) Draw and explain operation of sample and hold circuit using op-amp.