GBTU 21/12/12 (M)

Printed ges—7 **EEC501**

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 2117 **Roll No.** | | | | | | | | | | |

B.Tech.

(SEM. V) ODD SEMESTER THEORY EXAMINATION 2012-13

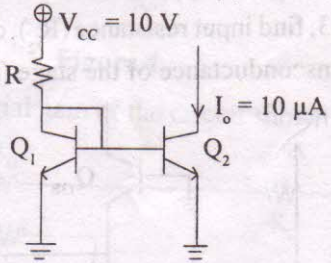
INTEGRATED CIRCUITS

Time : 3 Hours *Total Marks : 100*

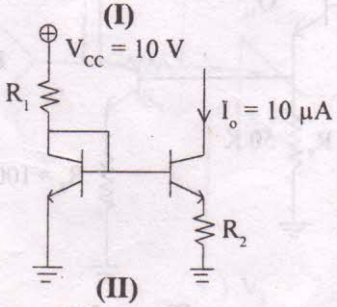
Note : *Attempt **all** questions. All questions carry equal marks. Assume missing data suitably if any.*

1. Attempt any **two** parts of the following : **(2×10=20)**

(a) Two circuits for generating constant current of 10 μA from 10 V power supply. Assuming all matched transistors, determine the value of resistances. Take V_{BE} = 0.7 V at 1 mA (Neglect effect of finite β).



(I)



(II)

Figure 1

Name the two circuits and compare their features as shown in Figure 1.

(b) Draw the circuit diagram of a Wilson current source and find the expression for current transfer ratio. For the circuit shown in Figure 2 below, find current transfer ratio.

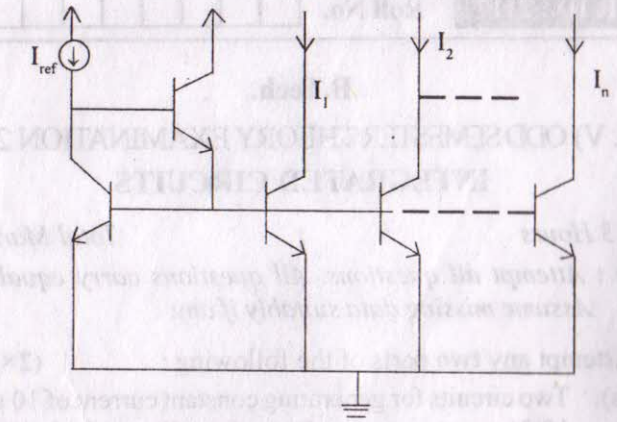


Figure 2

(c) Second stage of a typical OP-AMP is shown in following Figure 3, find input resistance (R_{i_2}), output resistance (R_{0_2}) and transconductance of the stage (G_{m_2}).

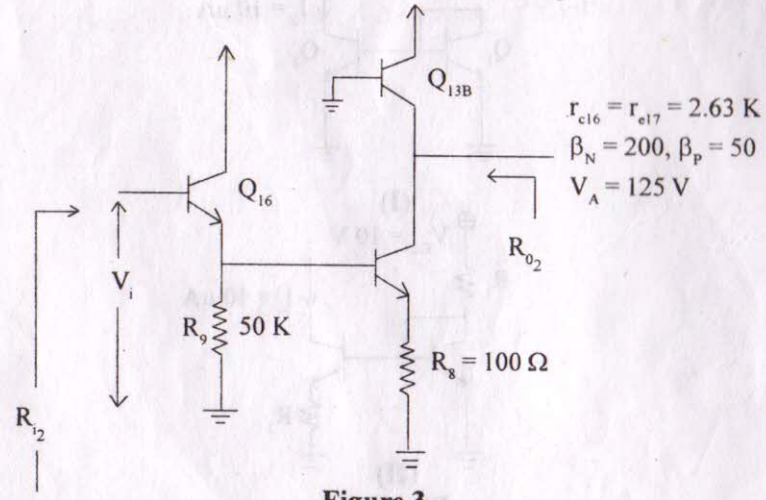


Figure 3

2. Attempt any **two** parts of the following : **(2×10=20)**

(a) For the circuit shown in Figure 4 show that common mode gain is minimum when $R_1 = R_3$ and $R_2 = R_4$.

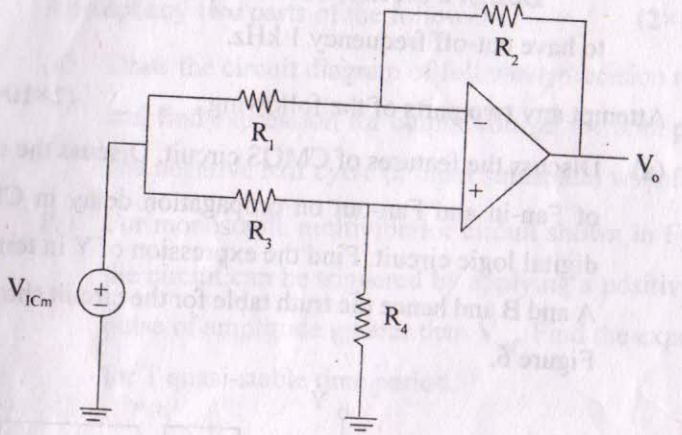


Figure 4

(b) Find differential gain of the circuit shown in Figure 5.

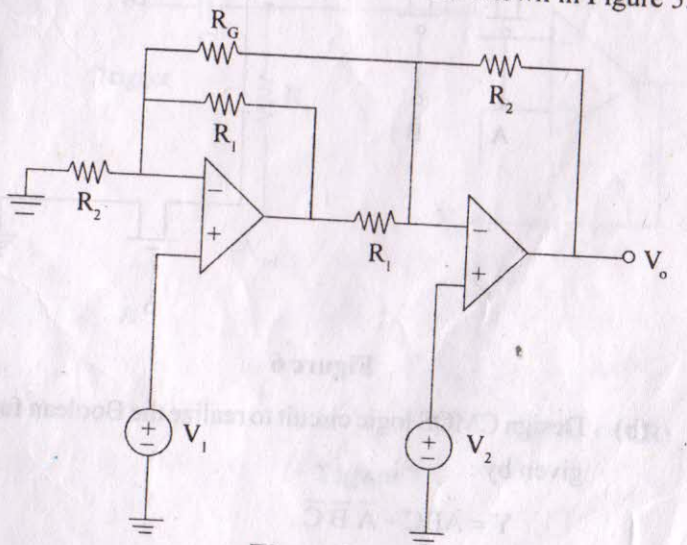


Figure 5

(c) Compare and contrast active filters and passive filters. Draw the circuit of II[nd] order low pass filters and find the expression for its cut-off frequency.

Design a second order low pass Butterworth filter to have cut-off frequency 1 kHz.

3. Attempt any **two** parts of the following : **(2×10=20)**

(a) Discuss the features of CMOS circuit. Discuss the effect of Fan-in and Fan-out on propagation delay in CMOS digital logic circuit. Find the expression of Y in terms of A and B and hence the truth table for the circuit shown in Figure 6.

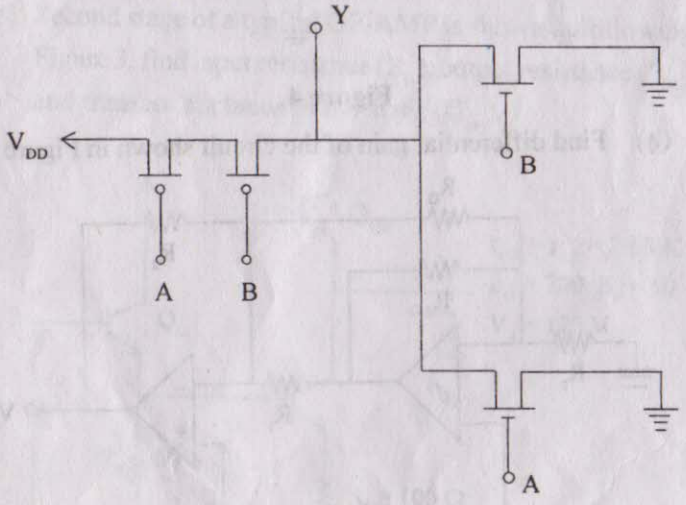


Figure 6

(b) Design CMOS logic circuit to realize the Boolean function given by :

$$Y = ABC + \overline{A}\,\overline{B}\,\overline{C}.$$

(c) Implement the following digital CMOS logic circuits :

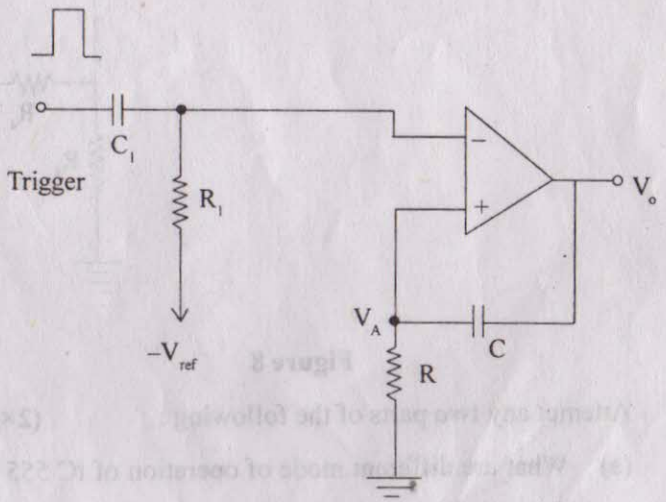
(i) S-R flip-flop

(ii) D Latch.

4. Attempt any **two** parts of the following : **(2×10=20)**

(a) Draw the circuit diagram of full wave precision rectifier and find expression for output voltage for both positive and negative half cycle of input sinusoidal waveform.

(b) For monostable multivibrator circuit shown in Figure 7 the circuit can be triggered by applying a positive input pulse of amplitude greater than V_{ref}. Find the expression for T quasi-stable time period.



$(C_1R_1 << CR)$

Figure 7

(c) For the circuit shown in Figure 8, show that output voltage is proportional to *ln* v_i (Assuming matched transistors).

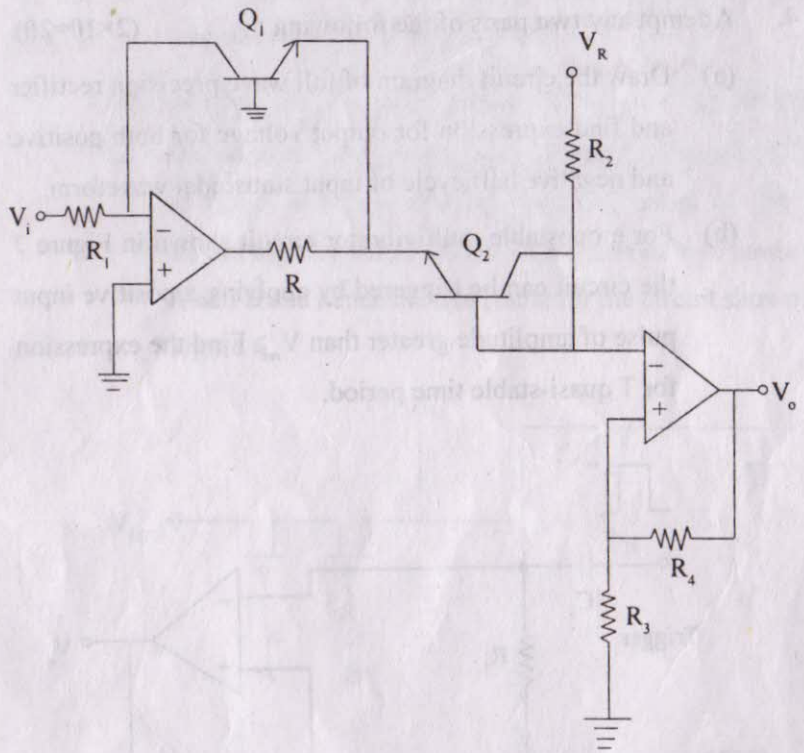


Figure 8

5. Attempt any **two** parts of the following : **(2×10=20)**

(a) What are different mode of operation of IC 555 ? Draw the circuit diagram of a delay circuit using 555. What is maximum delay that can be provided with 555 with a capacitor of 1000 μF ?

(b) Dra[illegible]he functional block diagram of PLL IC. Explain its working and deduce the expression for maximum frequency range of signal that can be locked.

(c) Draw the circuit diagram of weighted resistor digital to analog converter and find the expression of its output analog voltage.