

(Following Paper ID and Roll No. to be filled in your Answer Books)

Paper ID : 2289462

Roll No.

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## B.TECH.

Regular Theory Examination (Odd Sem - III), 2016-17

### SWITCHING THEORY AND LOGIC DESIGN

Time : 3 Hours

Max. Marks : 100

#### Section - A

1. Attempt all parts. All parts carry equal marks. Write answer of each part in short (10×2=20)
- Convert  $(153.513)_{10}$  to an octal number.
  - Write the advantages of gray code over the straight binary number sequence.
  - Give the general procedure for converting a multilevel AND-OR diagram into an all NAND diagram.
  - Draw the logic diagram of half subtractor.
  - Specify the purpose of valid bit indicator in priority encoder.
  - Give the function table of SR latch.
  - Express the characteristic equation for the JK flip-flop.

- h) Compare mealy and Moore model of finite state machine.
- i) The contents of a four bit register are initially 1011. The register is shifted six times to the right with serial input being 101111. What are the contents of the register after each shift?
- j) Write the steps that must be taken for the purpose of transferring a new word to be stored into memory.

**Section - B**

2. Attempt any five questions from this section

(5×10=50)

- a) Simplify the Boolean function.  

$$F(w, x, y, z) = \sum(1, 3, 7, 11, 15)$$
 Which has the don't care conditions  

$$d(w, x, y, z) = \sum(0, 2, 5)$$
- b) Implement the following Boolean function with NAND gates  

$$F(x, y, z) = \sum(1, 2, 3, 4, 5, 7)$$
- c) Design a full subtractor circuit with three inputs  $x, y$   $B_{in}$  and two outputs Diff and  $B_{out}$ . The circuit subtracts  $x - y - B_{in}$ , where  $B_{in}$  is the input borrow,  $B_{out}$  is the output borrow and Diff is the difference.
- d) Draw the logic diagram of a two to four line decoder using NOR gates only.

- e) Construct a JK flip-flop. using a D flip-flop. a two to four one line multiplexer and an inverter.
- f) Design a hazard free circuit for the following Boolean function  $F(x_1, x_2, x_3) = \sum(1, 5, 6, 7)$
- g) Describe the operation of four bit synchronous binary counter with neat sketch.
- h) Draw the basic configuration of three PLDs.

**Section - C**

Note: Attempt any two questions from this section.

(2×15=30)

- 3. Minimize the following switching function using Quine-McCluskey method  

$$F(x_1, x_2, x_3, x_4, x_5) = \sum(0, 1, 2, 8, 9, 15, 17, 21, 24, 25, 27, 31)$$
- 4. Design a combinational circuit that converts a BCD code to Excess-3 code.
- 5. Implement the following four boolean functions with a PAL.  

$$W(A, B, C, D) = \sum(2, 12, 13)$$

$$X(A, B, C, D) = \sum(7, 8, 9, 10, 11, 12, 13, 14, 15)$$

$$Y(A, B, C, D) = \sum(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$$

$$Z(A, B, C, D) = \sum(1, 2, 8, 12, 13)$$