

(Following Paper ID and Roll No. to be filled in your Answer Book)

Paper ID :131304

Roll No.

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B.Tech.

(SEM. III) THEORY EXAMINATION, 2015-16

SWITCHING THEORY & LOGIC DESIGN

[Time:3 hours]

[Total Marks:100]

Section-A

1. Attempt **all** parts. All parts carry equal marks. Write answer of each part in short. (10×2=20)
- (a) Write the difference between Decoder and Demultiplexer.
- (b) Perform the subtraction using 2's complement 46-23
- (c) Realize an EX-OR gate using NAND gates only.
- (d) How many address lines and data I/O lines are required for a 16K X 12 memory?
- (e) Simplify the following Boolean expression to a minimum number of literals:
- $$(x'y'+z)'+z+xy+wz$$
- (f) Differentiate between Asynchronous and Synchronous Sequential Circuits.

- (g) What are the required no. of flip flops in a MOD-16 Asynchronous Counter, MOD-16 Synchronous Counter, MOD-16 Ring Counter, MOD-16 Johnson Counter?
- (h) Design a Half Adder using Multiplexer.
- (i) Convert the decimal number 32.75 in Octal, Binary, Hexadecimal, Gray.
- (j) Draw Master Slave Flip-Flop.

### Section-B

Attempt any five questions from this section. (10×5=50)

- Design a 4-bit magnitude comparator using one bit comparator modules.
- Prepare hamming Code for the message "01001001010" assuming even parity. Also explain error detection and correction capabilities at the receiver by assuming an error in any of the received bits.
- Using a decoder and external gates, design the combinational circuit defined by the following three boolean functions:

$$F_1 = x'yz' + xz$$

$$F_2 = xy'z' + x'y$$

$$F_3 = x'y'z' + xy$$

- Design a 3-bit binary to Gray Code converter using PLA.
- Draw and explain 4-bit Universal shift register.
- Describe the hazards in digital Circuits. How are these removed?
- What do you understand by state reduction? Reduce the following state diagram.

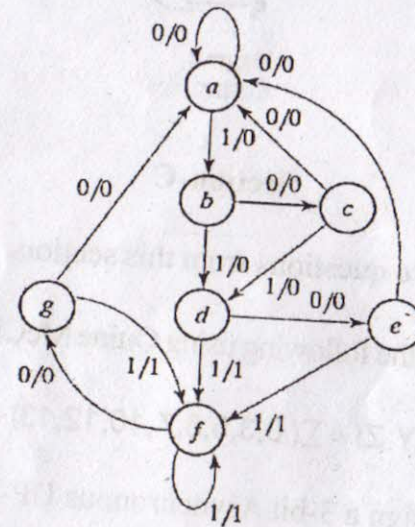


Figure 1

9. Derive the State Table and State Diagram for the sequential Circuit shown in figure 2:

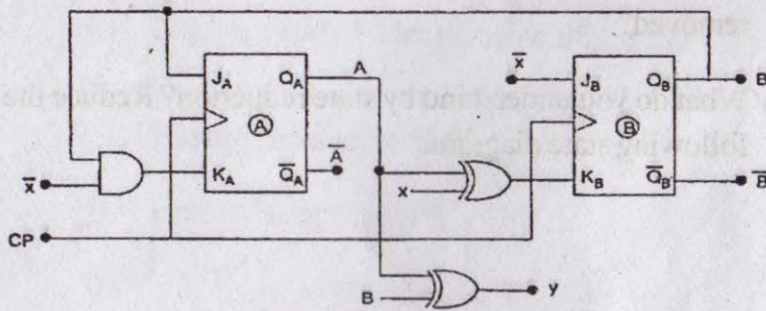


Figure 2

### Section-C

Attempt any two questions from this section. (15×2=30)

10. Minimize the following using Quine McCluskey method:

$$F(W, X, Y, Z) = \sum(0, 3, 5, 6, 7, 10, 12, 13) + \sum d(2, 9, 15)$$

11. (a) Design a 3-bit Asynchronous UP-Down Counter using T-Flip-Flop.  
 (b) Design a Full Adder using two Half Adders.

12. Design the clocked sequential circuit for the following state diagram using JK Flip-Flops.

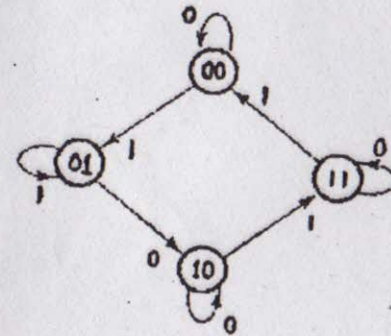


Figure 3

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