Section-C

Attempt **any two** questions from this section. $15 \times 2 = 30$

10. (a) Implement the following Boolean function with a multiplexer:

$$F(A, B, C, D) = \sum(0, 2, 5, 7, 11, 14)$$

(b) Using a decoder and external gates, design th combinational circuit defined by the following three Boolean functions:

$$F1 = (y'+x)z$$
$$F2 = y'z'+yz'$$
$$F3 = (x'+y)z$$

11. Minimize the following Boolean function using tabular method (Quine Mc- Cluskey method)

$f(A,B,C,D) \sum = m(4,5,6,8,9,10,13) + \sum d(0,7,15)$

12. A sequential circuit has two JK flip-flops A and B, two inputs X and Y, and one output Z. The flip-flop input equations are:

JA=BX+B'Y' KA=B'XY'

JB=A'X KB=A+XY'

Z=AXY+BX'Y'

a) Draw the logic diagram

b) Derive the state equations.

c) Obtain the state table, state diagram.

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(Following Paper ID and Roll No. to be filled in your Answer Book)

Paper ID :131305 Roll No. | | | | | | | | | | |

B.Tech.

(SEM. III) THEORY EXAMINATION, 2015-16

DIGITAL LOGIC DESIGN

[Time:3 hours] **[Total Marks:100]**

Section-A

1. Attempt **all** parts. All parts carry equal marks. Write answer of each part in short. $(10 \times 2 = 20)$

(a) Define Primitive Flow table.

(b) What is race around condition in JK flip flop?

(c) How many address lines and input output lines are needed in 2G X8 memory unit.

(d) Differentiate between EPROM and EEPROM.

(e) Design full adder using two half adders.

(f) Differentiate between encoders and decoders.

(g) Subtract 11010 from 10110 using 2's complement.

(h) Represent $(213.25)_{10}$ insingle precision floating point representation.

(i) Convert decimal 9 into gray code.

(j) Simplify the Boolean expresion: Y=(A+B) (A+C') (B'+C').

Section-B

Attempt **any five** questions from this section. (10×5=50)

2. Obtain Hamming codeward for the given data: "11001001010"

3. Design a4-bit by 4-bit Binary Multiplier.

4. Design a 3-bit binary to Gray Code converter using PLA.

5. Explain the difference between SRAm and DRAM.

6. Draw and explain 4-bit Universal shift Register.

7. Design a clocked sequential circuit that operates according to the state diagram shown:

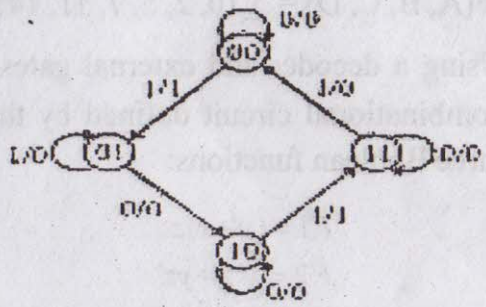

Figure: State Diagram

Implement the circuit using D Flip-Flop.

8. Describe the general procedures that must be followed to ensure a face-free state assignment with example.

9. Obtain the reduced flow table for an Asynchronous sequential circuit that has two inputs x2 and x1 and one output z. When x1=0 the output z=0. The first change in x2 that occurs while x1=1 will cause output z to be 1. The output z will remain 1 until x1 returns to zero.