

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3072

Roll No.

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**B. Tech.**

(SEM. III) ODD SEMESTER THEORY EXAMINATION  
2010-11

**SWITCHING THEORY***Time : 3 Hours**Total Marks : 100***Note : Attempt all the questions. All questions carry equal marks.**

1. Attempt any **four** parts of the following : (5×4=20)
  - (a) Convert binary 11010111.110 to decimal, octal and hexadecimal.
  - (b) Subtract 61 from 68 using BCD. Also show all the necessary steps.
  - (c) Using Tabular method and algebraic solution of P.I. table, obtain minimal realization of a function shown below :  
$$F(A, B, C, D, E) = \sum m(13, 15, 17, 18, 19, 20, 21, 23, 25, 27, 29, 31) + \sum d(1, 2, 12, 24).$$
  - (d) How does parity help in error-detection ? Explain.
  - (e) Using boolean postulates, prove DeMorgan's theorem.
  - (f) What are universal gates ? Why they called so ? Explain with example.
  
2. Attempt any **four** parts of the following : (5×4=20)
  - (a) Design a full subtractor.
  - (b) Design a 4-bit magnitude comparator.
  - (c) Design a binary to Gray code converter.



- (d) Design a full adder with a decoder and OR-gates.
- (e) A ROM is to be used to implement the boolean functions :

$$F_1(A, B, C, D) = ABCD + \bar{A}\bar{B}\bar{C}\bar{D}$$

$$F_2(A, B, C, D) = (A + B) + (\bar{A} + \bar{B} + C)$$

$$F_3(A, B, C, D) = \Sigma m(13, 15) + \Sigma d(3, 5)$$

What is the minimum size of the ROM required ?

- (f) Implement the following functions using PLA :

$$F_1 = A\bar{B} + AC$$

$$F_2 = AC + BC$$

3. Attempt any **two** parts of the following : (10×2=20)

- (a) (I) Convert a D-FF to a T-FF.
- (II) Draw a neat diagram of master slave JK FF. Explain how race around condition is avoided using master-slave JK flip-flop.
- (b) (I) Design a universal shift register.
- (II) Draw the ASM chart for a binary multiplier.
- (c) Design a JK flip-flop asynchronous sequential circuit that has two inputs and single output. The circuit is required to give an output equal to 1 if and only if the same input variable changes two or more times consecutively.

4. Attempt any **four** parts of the following : (5×4=20)

- (a) Explain the AC noise margin and DC noise margin.
- (b) What is CMOS ? Why its use in digital circuit is advantageous ?
- (c) Why FAN OUT of ECL is higher and propagation delay is lower ?

Explain the interfacing of CMOS to TTL logic gate.

- (e) With the help of circuit diagram explain CMOS inverter.
- (f) What is three state logic ? Draw the circuit diagram of three state NAND gate and explain its operation.

5. Attempt any **four** parts of the following : (5×4=20)

- (a) Define Hazard and find the hazard free realization of the combinational circuit :

$$Y = A\bar{B} + BD$$

- (b) Discuss the fault table method for fault detection in digital circuit.
- (c) Given two 2K × 8 ROM ICs and two 2K × 8 RAM ICs. Obtain a memory system of 8K × 8 bits.
- (d) With the help of diagram, explain the operation of a bipolar SRAM cell.
- (e) Explain how a multiplexer can be used as ROM ?
- (f) Explain the basic structure of a EPROM cell ? Why they are so popular ?