Calculate the value of R_C required for the open collector gate. Assume $V_{CC} = 5\,V$ and a fan out of 8.

(c) Compare the current spikes in ECL and TTL gates.

5 Attempt any **two** of the following : **10×2=20**

(a) Obtain a 16×8 memory using 16×4 memory ICs draw the concerned IC circuit.

(b) Explain : Linear selection addressing.

(c) Draw circuit for

One-bit dynamic NMOS cell and explain the operation of a dynamic MOS inverter.

* 3 0 7 2 / 2 1 0 1 0 *

Printed Pages : 4 TEC-302

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3072 Roll No.

B. Tech.

(SEM. III) EXAMINATION, 2007-08

SWITCHING THEORY

Time : 3 Hours] *[Total Marks : 100*

Note : (1) All questions carry equal marks.

(2) Attempt all questions.

1 Attempt any four of the following : **5×4=20**

(a) Make a K-map for the function

$$f = AB + A\bar{C} + C + AD + A\bar{B}C + ABC$$

(1) Express f in standard SOP form

(2) Minimize it and realize the minimized expression using NAND gates only.

(b) Design Excess-3 to BCD code converter using minimum number of NAND gates.

(c) A line printer is capable of printing 132 characters in a single-line and each character is represented by ASCII code. How many bits are required to print each line ?

(d) Prove the following :

(1) $A \oplus B = \overline{A} + \overline{B}$

(2) $B \oplus (B \oplus A \cdot C) = A \cdot C$

(e) For the logic expression $Y = A\overline{B} + \overline{A}B$

(1) Realize this using AND, OR, NOT gates and

(2) Realize using NAND gate only.

(f) Determine Hamming code sequence with odd parity for natural BCD for making it an error correcting code.

2 Attempt any four of the following : **5×4=20**

(a) Design a parity generator to generate an odd parity bit for a 4-bit word. Use EX-OR and $\overline{\text{EX-OR}}$ gate.

(b) Design a full adder circuit using two half adders.

(c) Develop 32:1 multiplexer using two 16:1 multiplexer and one 2:1 multiplexer.

(d) Present an algorithm for performing subtraction using adder.

(e) Implement the expression using a multiplexer

$$f(A, B, C, D) = \Sigma m(0, 2, 3, 6, 8, 9, 12, 14)$$

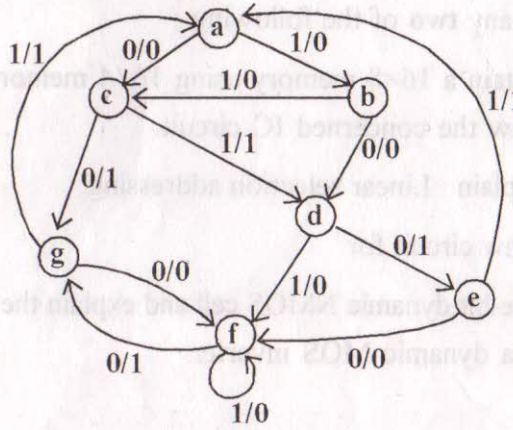
(f) Design a BCD-to-seven segment decoder using a PLA.

3 Attempt any two of the following : **10×2=20**

(a) Describe and discuss the operation of a D-type flop-flop.

(b) Design a 3-bit synchronous counter using J-K flip-flops.

(c) Design a docked sequential circuit for the state diagram.



4 Attempt any **two** of the following : **10×2=20**

(a) Draw and explain "an output circuit arrangement" for explaining "active pull-up" in TTL gates.

(b) For an open collector TTL gate, the specifications are

$V_{OH} = 2.4\ V$

$V_{OL} = 0.4\ V$

$I_{OH} = 250\ \mu A$

$I_{OL} = 16\ mA$

$I_{IH} = 40\ \mu A$

$I_{IL} = -1.6\ mA$