(b) What is the basic architecture of a PLA ? How is the capacity of a PLA specified ? How is it programmed ? Explain.

(c) Draw the logic configuration of four input and four output PAL and explain.

5. Attempt any **two** parts of the following : **(10×2=20)**

(a) Differentiate between asynchronous and synchronous sequential circuit. Define fundamental mode of operation.

(b) Define critical race and non-critical race. Discuss the concept of non critical race with examples.

(c) Describe briefly the excitation table and output table of a fundamental mode asynchronous sequential circuit.

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0323 Roll No.

B.Tech.

(SEM. III) THEORY EXAMINATION 2011-12

DIGITAL ELECTRONICS

Time : 3 Hours *Total Marks : 100*

Note :– Attempt **all** questions. Each question carries equal marks.

1. Attempt any **four** parts of the following : **(5×4=20)**

(a) Represent decimal number "–13" in all four methods of negative binary number representation using eight bits.

(b) Perform the following subtraction using 2's complement method :

(i) 01000–01001

(ii) 0011.1001–0001.1110

(c) Add the following numbers :

(i) $(ABC)_{16} + (CDE)_{16}$

(ii) $(77)_8 + (107)_8$

(d) Detect and correct error (if any) in the following received even parity Hamming code word 00111101010. Also find out the correct message.

(e) Minimize the given Boolean function using K-Map and implement the simplified function using NAND gates only.
$F(A, B, C, D) = \Sigma m(0,1,2,9,11,15) + d(8,10,14)$.

(f) Minimize the following function using Quine Mc Clusky method :
$f(A, B, C, D) = \Sigma m(0,2,3,6,7,8,9,10,13)$

2. Attempt any **two** parts of the following : **(10×2=20)**

(a) Construct a BCD to excess 3 code converter with a 4 bit adder. What must be done to change the circuit to an excess 3 to BCD code converter ?

(b) What is magnitude comparator ? Design a three bit comparator circuit using logic gates.

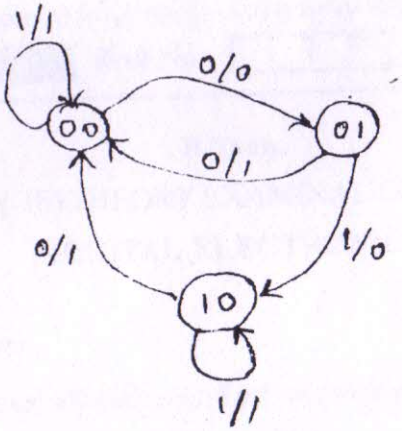
(c) (i) Design a full subtractor circuit with a decoder and two OR gates.

(ii) Implement the function :
$F(A,B,C) = \bar{A}\,\bar{B}\,C + \bar{A}\,B\bar{C} + A\bar{B}\bar{C} + ABC$ using 4 : 1 multiplexer using A and B variables to the selection lines.

3. Attempt any **two** parts of the following : **(10×2=20)**

(a) Draw RS flip-flop and write the characteristic table and characteristic equation for it. Explain how will you convert it into D flip-flop.

(b) Design a circuit that implements the state diagram.



(c) Design a synchronous counter using J-K flip-flop for the following input sequences :

A	B	C
0	0	0
0	0	1
0	1	0
1	0	0
1	0	1
1	1	0
0	0	0

4. Attempt any **two** parts of the following : **(10×2=20)**

(a) What is ROM ? What are the various types of ROM ? Explain.