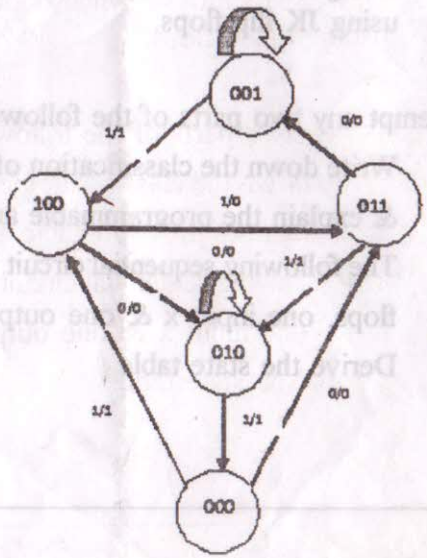

Fig 2

5. Attempt any two parts of the following : **10×2=20**

(a) An asynchronous sequential circuit has two internal states & one output. The excitation functions and output function of the circuit as follows:

$Y_1 = \bar{x}_1 x_2 + x_2 y_1$

$Y_2 = x_1 y_2 + x_2$

Output function

$z = x_1 + y_2$

(i) Realize the logic diagram of the circuit.

(ii) Derive the transition table & output map.

(b) Define Hazards, Races & Cycles in asynchronous sequential circuits.

(c) Explain realization of ASM chart using multiplexer.

Printed Pages : 4

ECS-301

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 110301

Roll No.

B. Tech.

(SEM. III) (ODD SEM.) THEORY EXAMINATION, 2014-15

DIGITAL LOGIC DESIGN

Time : 3 Hours] [Total Marks : **100**

Note : Attempt all questions. Each question carry equal marks.

1. Attempt any four parts of the following : **5×4=20**

(a) Perform the following arithmetic using 2's complement

(i) 14–22 (ii) –22+17

(b) Write the standard SOP & POS form of the following functions

(i) $F(A,B,C) = \bar{A} + BC + AB\bar{C}$

(ii) $F(A,B,C) = (A+B+C)(A+\bar{B}+\bar{C})(\bar{A}+B+D)$

(c) Write a short note on Weighted & Non-weighted binary codes.

(d) Simplify the following Boolean Expression using 5 variable K-Map.

$F(a,b,c,d,e) = \Sigma\, m(1,3,7,11,15,17,19,23,27,31) + \Sigma\, d(0,2,5,16,18,21)$

(e) Determine the error position in the received odd parity hamming code 01011101011. Give corrected data.

(f) Minimize the following Boolean expression using Tabular Method.

$F(w,x,y,z)= \Sigma m(1,3,4,5,6,8,9,10,11)$

2. Attempt any four parts of the following : **5×4=20**

(a) Implement a 16×1 multiplexer using 4×1 multiplexers.

(b) Implement the following Boolean function with 4×1 Multiplexer

$F(A,B,C,D)=\Sigma m(0,2,4,5,6,7,9,11,12,14)$ control variables are C & D.

(c) Design an even & odd parity generator. Assume the input to be three bit binary words.

(d) Implement the following function using a suitable decoder $F(x,y,z)=x\ y\ z' + x'z$

(e) Design a combinational circuit for a BCD to Gray Code Converter.

(f) Design a combinational circuit with three inputs x,y,z & three outputs A,B,C such that when binary input is 0,1,2,3, the binary output is one greater than the input & when the binary input is 4,5,6,7, the binary output is one less than the output.

3. Attempt any four parts of the following : **5×4=20**

(a) Obtain T flip-flop from S-R flip- flop.

(b) Obtain the Characteristic equation for JK flip flop

(c) Design Modulo-3 synchronous up counter using S-R flip flop

(d) Explain the operation of a universal shift register using D flip flops & multiplexers.

(e) Explain J K Flip-flop using NOR Gates. Explain Race Around condition.

(f) Design Modulo-5 Asynchronous binary up counter by using JK flip flops.

4. Attempt any two parts of the following : **10×2=20**

(a) Write down the classification of memories. Also draw & explain the programmable array logic.

(b) The following sequential circuit in fig 1 has two JK flip flops, one input x & one output y.

Derive the state table

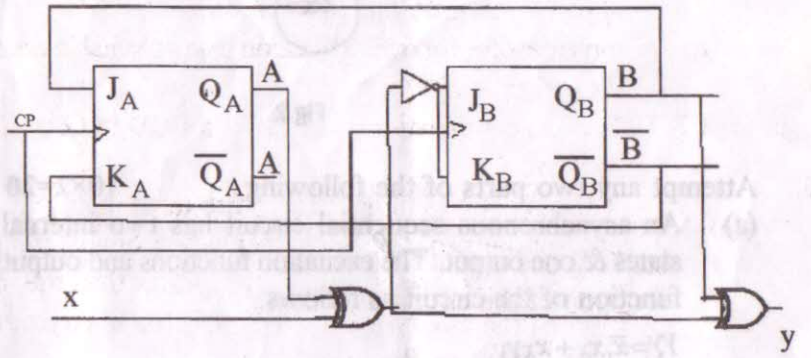

Fig 1

(c) Design a sequential circuit that has three JK flip flops A,B,C, one input x and one output y.

The state diagram is given in fig 2. The circuit is to be designed by treating the unused states as don't care conditions.