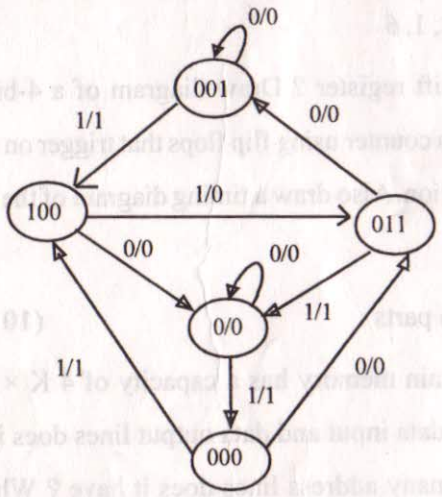
5. Answer any **two** parts : (10× 20)

(a) A sequential circuit has one input and one output. The state diagram is shown in following figure :



Design the sequential circuit with T flip-flops.

(b) A sequential circuit has four flip-flops A, B, C, D and an input x. It is described by following state equations :

$A(t+1) = (C D' + C' D) x + (CD + C'D') x'$

$B(t+1) = A$

$C(t+1) = B$

$D(t+1) = C.$

(i) Obtain the sequence of states when x = 1 starting from ABCD = 0001.

(ii) Obtain the sequence of states when x = 0 starting from ABCD = 0000.

(c) Write short notes on any **two** of the following :

(i) Asynchronous sequential logic versus Synchronous sequential logic.

(ii) Hazards in combinational and sequential circuits.

(iii) State reduction in sequential circuits.

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0109 **Roll No.**

B. Tech.

(SEM. III) THEORY EXAMINATION 2011-12

DIGITAL LOGIC DESIGN

Time : 3 Hours *Total Marks : 100*

Note :– Answer **all** questions.

1. Answer any **four** parts : **(5×4=20)**

(a) How can functionalities of the OR gate be realized using only NAND gates ?

(b) Simplify following boolean expressions :

(i) $A + A'B + A'B' C + A'B'C' D + A'B'C'D'E + A'B'C'D'E'F$

(ii) $D (A'+B) + B' (C+AD)$

(c) What is Hamming Code ? How it is used for detecting and correcting errors ? Explain with the help of suitable example.

(d) Express the following boolean function F in a sum of minterms and a product of maxterms :

$F(x, y, z) = (xy + z) (y + xz)$

(e) Simplify the boolean function G using the don't care conditions d using Karnaugh map :

$G = A' B' D + A' CD + A' B C$

$d = A' BC' D + ACD + A B'D'$

(f) (i) Convert the decimal number 25.2 to binary number.

(ii) Perform following arithmetic operation in binary using signed 2' complement representation :

(–42) – (–13)

2. Answer any **four** parts : **(5×4=20)**

(a) Design a logic circuit whose output is 1 only when a majority of inputs A, B, C are 0.

(b) Implement a full subtractor with two half subtractors and an OR gate.

(c) Implement the following boolean function F using three half adder circuits :

$F(A, B, C) = A \oplus B \oplus C$.

(d) Design a combinational circuit that compares the magnitude of two 4 bit numbers and its output indicates whether $A > B$, $A = B$ or $A < B$.

(e) What is multiplexer ? Give implementation of a full adder circuit using 4×1 multiplexers.

(f) What is priority encoder ? Explain with the help of suitable example.

3. Answer any **two** parts : **(10×2=20)**

(a) (i) What is flip-flop ? Draw the logic diagram and give the characteristic table of J K flip-flop.

(ii) Explain the race condition in context of RS flip-flop.

(b) Design a binary counter using J K flip-flops having the following repeated sequences :

0, 4, 2, 1, 6

(c) What is shift register ? Draw diagram of a 4-bit binary ripple down counter using flip flops that trigger on negative edge transition. Also draw a timing diagram of the counter.

4. Answer any **two** parts : **(10×2=20)**

(a) (i) A certain memory has a capacity of 4 K × 8. How many data input and data output lines does it have ? How many address lines does it have ? What is its capacity in Bytes ?

(ii) Discuss the following types of ROM, PROM, EPROM, EEPROM.

(b) (i) Design a 16×8 memory using 16×4 memory units.

(ii) Differentiate between programmable array logic (PAL) and programmable logic assays (PLA).

(c) (i) Draw the logic diagram of 4 input multiplexer. Further show how 4-input multiplexer can be realized using 2-input multiplexers.

(ii) Draw the logic diagram of one line to 8-line demultiplexer.