5. Attempt any **two** questions of the following :

(a) Discuss various models of computation in PRAM (Parallel Random Access Machine) model. Also explain how theoretically parallel algorithms are analysed.

(b) Devise a PRAM algorithms to sort a given array of an element using bubble sort.

(c) Discuss matrix multiplication on mesh. Give an algorithm that uses n × n processors arranged in a mesh configurations. Also find the time complexity of the algorithm.

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0148 **Roll No.**

B.Tech.

(SEM. VIII) THEORY EXAMINATION 2010-11

ADVANCE COMPUTER ARCHITECTURE

Time : 3 Hours *Total Marks : 100*

Note : (1) Attempt **all** questions.

(2) All questions carry equal marks.

(3) Assume suitable data wherever necessary.

1. Attempt any **two** parts of the following :

(a) Explain Flynn's classification of computer architecture and how it is different from Feng's classification ?

(b) In the following program segment, detect if parallelism is possible using Bernstein's conditions :

S_1 : $A = B * C ; A \leftarrow B \times C$

S_2 : $C = D * E ; C \leftarrow D * E$

S_3 : $G = F + G ; G \leftarrow F + G$

S_4 : $H = G + A ; H \leftarrow G + A$

(c) Draw a 16 bit omega network using 2×2 switches as building block.

2. Attempt any **two** parts of the following :

(a) A nonpipeline system takes 50 ns to process a task. The same task can be processed in a 6 segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speed-up that can be achieved ?

(b) What are pipeline hazards ? Discuss various branch prediction strategies with the help of examples.

(c) What do you understand by control flow and data flow computers ? State advantages and disadvantages of data flow computing ?

3. Attempt any **two** parts of the following :

(a) A block set associative cache consists of a total 64 blocks divided into four-block sets. The main Memory contains 4096 blocks. Each block consists of 128 words.

(i) How many bits are there in Main Memory address ?

(ii) How many bits are there in each of TAG, SET and WORD fields of Main Memory.

(b) Suppose in a memory organisation, cache miss rate is 5%. The cache memory has cycle time of 20 ns whereas main memory has cycle time of 150 ns. Calculate the average cycle time.

(c) Explain the temporal locality, spatial locality and sequential locality associated with program/data access in a memory hierarchy ?

4. Attempt any **two** parts of the following :

(a) Consider the following reservation table for a four stage pipeline with a clock cycle $\tau = 20$ ns.

	1	2	3	4	5	6
S_1	X					X
S_2		X		X		
S_3			X			
S_4				X	X	

(i) What are forbidden latencies and initial collission vector ?

(ii) Determine MAL associated with the shortest greedy cycle.

(b) In a given architectural configuration of SIMD computers, discuss how data -routing mechanisms are implemented.

(c) Discuss the superscalar and superpipelined processing. Also estimate the performance of superpipelined superscalar processor of degree (m, n).