

5. Attempt any two parts of the following :

- (a) Consider the following reservation table for a four stage pipeline with a clock cycle $t_c = 20\text{ns}$.

	1	2	3	4
S1	X			X
S2		X		
S3			X	

- (i) What are the forbidden latencies and initial collision vector ?
 - (ii) Draw the state transition diagram for scheduling the pipeline.
 - (iii) List all the simple cycle and greedy cycle.
 - (iv) Determine the optimal constant latency and minimal average latency (MAL).
 - (v) Determine the throughput of this pipeline. Lower bound on the MAL for this pipeline.
- (b) What are the properties of the Vector Processors ? Explain each component of Vector-Register Processors with diagram.
- (c) Discuss the superscalar and superpipelined processing. Also estimate the performance of superpipelined superscalar processor of degree (m, n).

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(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0148 Roll No.

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B.Tech.

(SEM VIII) EVEN SEMESTER THEORY EXAMINATION,
2009-2010

ADVANCED COMPUTER ARCHITECTURE

Time : 3 Hours

Total Marks : 100

1. Attempt any two parts of the following :

- (a) Analyse the data dependencies among the following statements in a given program :

S1 : Load R1, 1024 /R1 ← 1024/
 S2 : Load R2, M(10) /R2 ← Memory (10) /
 S3 : Add R1, R2 /R1 ← (R1) + (R2) /
 S4 : Store M(1024), R1 /Memory (1024) ← (R1) /
 S5 : Store M(R2), 1024 /Memory (64) ← 1024 /

Note that (R_i) means that the content of register R_i and Memory (10) contains 64 initially.

- (i) Draw a dependence graph to show all the dependencies.
 - (ii) Are there any resource dependencies if only one copy of each functional unit is available in the CPU ?
- (b) Explain the types of system performance factors in a parallel architecture.
- (c) Draw a 16 bit omega network using 2 × 2 switches as building block.

2. Attempt any two parts of the following :

- (a) Consider n level hierarchical memory, let ' h_i ' be hit ratio at level M_i . Show that access frequency to ' M_i ' is given by :

$$f_i = (1-h_1) (1-h_2) \dots (1-h_{i-1}) \cdot h_i$$

Further show that effective access time :

$$T_{\text{eff}} = \sum f_i t_i$$

here ' t_i ' are measured with respect to CPU.

- (b) Compare and contrast static interconnection network and dynamic interconnection network ?
- (c) What do you mean by control flow and Data flow computers ? State advantage and disadvantage of data flow computing.

3. Attempt any two parts of the following :

- (a) Explain the Flynn's classification for Computer Architectures based on the nature of the instruction flow executed by the computer with diagram.
- (b) What does an array processor mean ? What are the different SIMD computer organizations ?
- (c) Vectorizing compilers generally detect loops that can be executed on a pipelined vector computer. Are the vectorization algorithms used by vectorizing compilers suitable for MIMD machine parallelization.

4. Attempt any two parts of the following :

- (a) A hierarchical cache main memory subsystem has following specifications :
- (i) Cache access time of 50 n sec
 - (ii) Main storage access time of 500 n sec
 - (iii) 80% of request are for read
 - (iv) Hit ratio of 0.9 for read access and for write through scheme is used,

Determine :

- (A) Average access time of the system considering only memory read cycle
 - (B) Average access time of the system both for read and write requests
 - (C) Hit ratio taking into considerations the write cycle
 - (1) 100 n sec
 - (2) 180 n sec
 - (3) 0.72 n sec
- (b) What are the different hazards that occur in instruction pipeline and how these are resolved ?
- (c) What is meant by Cache-Coherency ? Explain with the help of a suitable example.