(ii) Hit Ratio

(iii) Associative memory

(iv) Virtual memory.

(c) Explain various cache mapping techniques. A 2-way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from the main memory. The main memory size is 128 K × 32.

(i) Formulate all pertinent information required to construct the cache memory.

(ii) What is the size of the cache memory ?

5. Attempt any **two** of the following : **(2×10=20)**

(a) Explain Asynchronous data transfer using both strobepulse and handshaking. Support your answer with Block Diagram, Tuning Diagram and Sequence of Events.

(b) Write short notes on following :

(i) Programmed I/O.

(ii) Interrupt Initiated I/O.

(c) Explain the working of DMA controller.

24/5/13

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0110 Roll No.

B.Tech.

(SEM. IV) EVEN THEORY EXAMINATION 2012-13

COMPUTER ORGANIZATION

Time : 3 Hours *Total Marks : 100*

Note :– Attempt **all** questions.

1. Attempt any **four** of the following : **(4×5=20)**

(a) What do you mean by overflow ? Describe the overflow detection.

(b) Explain various methods of bus arbitration. Write the advantages and disadvantages of daisy chaining method.

(c) Convert the following decimal numbers to the bases indicated :

(i) 7625 to Octal

(ii) 1983 to Hexa decimal

(iii) 174.5 to Binary

(iv) 6279 to Octal

(v) 3001 to Hexa decimal.

(d) Represent $(1460.125)_{10}$ in Single Precision and Double Precision formats.

(e) Show the hardware that implements the following statements. Include the logic gates for the control function

and a block diagram for the binary counter with a count enable input.

$$xy\,T_0 + T_1 + y'\,T_2 : AR \leftarrow AR + 1$$

(f) Define the significance of Hamming Code with example.

2. Attempt any **two** of the following : **(2×10=20)**

(a) Explain Booth's algorithm with its flow chart and hardware configuration.

Multiply (–7) and (+3) using Booth's algorithm. Convert into binary equivalent.

(b) Write a program to evaluate the arithmetic statement

$X = (A + B * C)/ (D – E/F)$

(i) Using general register computer with 3-address instruction.

(ii) Using general register computer with 2-address instruction.

(iii) Using an accumulator type computer with 1-address instruction.

(iv) Using a stack organized computer with 0-address operation instruction.

(c) Determine the micro operations that will be executed in a system having 7 register, ALU and 2 multiplexers of size 8×1 each, when the following 14-bit control words are applied.

(i) 00101001100101

(ii) 00000000000000

(iii) 01001001001100

(iv) 00000100000010

(v) 11110001110000

3. Attempt any **two** of the following : **(2×10=20)**

(a) What is interrupt cycle ? Write short note on interrupt types.

(b) Explain Hardwired and Microprogrammed control and compare them.

(c) Write short notes on :

(i) Instruction cycle

(ii) RISC

(iii) CISC.

4. Attempt any **two** of the following : **(2×10=20)**

(a) A computer employs RAM chips of 256 × 8 and ROM chips of 1024 × 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM and 4 interface unit each with 4 registers. A memory mapped configuration in used. The 2-highest order bits of address bus are assigned '00' for RAM, '01' for ROM and '10' for interface registers.

(i) How many RAM and ROM chips are needed ?

(ii) Draw a memory address map for the system.

(iii) Give the address range in hexadecimal for RAM, ROM and interface.

(b) Write short notes on following :

(i) Locality of reference