

1st Aug, 2017

**KRISHNA ENGINEERING COLLEGE**

**ELECTRONICS & COMMUNICATION ENGINEERING DEPARTMENT**

**SKILL DEVELOPMENT COURSES**

Electronics & Communication Engineering Department is offering following courses for Skill Development. The classes will be conducted on working Saturdays. Interested students may give their name to the coordinators by 7 Aug 2017.

S.No.	Course Name	Designed for	Time period	Coordinator	Objective
1	Digital Image Processing using MATLAB	ECE 3 <sup>rd</sup> year	30 hrs	Sakshi Gupta & Radhika Goel	To provide hands on experience on image analysis.
2	VHDL & Schematic Design using ORCAD & Xilinx	ECE 3 <sup>rd</sup> year	30 hrs	Deepali Garg, Sangeeta Patel & Malti Gautam	To learn the designing of an IC using VHDL.

The details of each course are mentioned in separate notices of each course. Students have to submit Rs. 500 as registration charges which will be refunded after successful completion of the course. A certificate will be provided to all participants and prizes will be given to top performing students.

**Prof. Dr. A.N. Mishra**

**HOD (ECE)**

## Krishna Engineering College, Ghaziabad

Electronics and Communication Department

### SKILL DEVELOPMENT COURSES

#### Digital Image Processing using MATLAB

##### **Course Description**

This course provides hands-on experience on image analysis. Examples and exercises demonstrate the use of appropriate MATLAB and Image Processing Toolbox functionality throughout the analysis process.

**Lab Required-** CAD Lab

##### **Software Tools**

- MATLAB Image Processing Toolbox

**Coordinators-** Ms. Sakshi Gupta & Ms. Radhika Goel

**Max Student Capacity-** 20 Students

**Applicable-** 3<sup>rd</sup> yr. Students

**Duration-** 30 hrs.

##### **Who Should Attend?**

Engineers who wish to enhance their skills in the field of Image & Video processing and apply their skills in designing a project.

##### **Prerequisites**

MATLAB Fundamentals.

##### **Skills Gained**

*After completing this training, you will know how to:*

- Import images into MATLAB
- Extract object details such as size and color to find subsequent image processing steps.
- Preprocess images by filtering and using contrast adjustment.
- Segment edges of objects and extract boundary pixel locations.
- Segment objects on the basis of their color & texture.
- Analyze and modify the objects shape to improve segmentation results. Count the detected objects.
- Simulate a basic Image Processing design and extract an object from the image.

**Digital Image Processing Workshop Schedule**

<b>Date</b>	<b>Topics</b>	<b>Description</b>
Session-1	1. Introduction of Image Processing Toolbox in MATLAB 2. Interactive Exploration of Images	Import images into MATLAB and visualize them. Convert the images to a format that is useful for subsequent analysis steps. <ul style="list-style-type: none"> <li>• Importing and displaying images</li> <li>• Converting between image types</li> <li>• Exporting images</li> </ul> Interactively explore object details such as size and color to find start values for subsequent image processing steps. <ul style="list-style-type: none"> <li>• Obtaining pixel intensity values</li> <li>• Extracting a region of interest (ROI)</li> <li>• Computing pixel statistics on a region of interest</li> <li>• Measuring object sizes</li> <li>• Creating a custom interactive tool</li> </ul>
Session-2	Preprocessing Images	Preprocess images by filtering, and using contrast adjustment to simplify or allow for image analysis steps. <ul style="list-style-type: none"> <li>• Adjusting image contrast</li> <li>• Reducing noise in an image by filtering</li> <li>• Handling in homogenous background</li> </ul>
Session-3	1. Edge and Line Detection 2. Feature Extraction	Segment edges of objects and extract boundary pixel locations. Detect lines and circles in an image. <ul style="list-style-type: none"> <li>• Segmenting object edges</li> <li>• Detecting straight lines</li> <li>• Performing batch analysis over sets of images</li> <li>• Detecting circular objects</li> </ul> Analyze and modify the objects shape to improve segmentation results. Count the detected objects and calculate object features like area or centroids. <ul style="list-style-type: none"> <li>• Counting objects</li> <li>• Measuring shape properties</li> <li>• Using morphological operations</li> <li>• Performing watershed segmentation</li> </ul>
Session-4	Color and Texture Segmentation	Segment objects based on color or texture. Use texture features for image classification. <ul style="list-style-type: none"> <li>• Color space transformation</li> <li>• Color segmentation</li> <li>• Texture segmentation</li> <li>• Texture-based image classification</li> </ul>

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Session-5	Mini Project	Students will be designing one of the following Mini Projects: <ul style="list-style-type: none"><li>• Character Recognition</li><li>• Gesture Based Mouse Pointer</li><li>• Count number of Object of same type</li></ul>
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**Each session is of 6 hrs.**

**Coordinators-  
Ms. Sakshi Gupta  
Ms. Radhika Goel**

**HOD (ECE)  
Dr. A. N. Mishra**

# Krishna Engineering College, Ghaziabad

## Electronics and Communication Department

### Xilinx Workshop

### SKILL DEVELOPMENT COURSES

### Designing in VHDL & ORCAD using XILINX

#### Course Description

This comprehensive course is a thorough introduction to the VHDL language. The emphasis is on writing solid synthesizable code and enough simulation code to write a viable test bench. Structural, register transfer level (RTL), and behavioral coding styles are covered. This class addresses targeting Xilinx devices specifically and FPGA devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course combines insightful lectures with practical lab exercises to reinforce key concepts. You will also learn best coding practices that will increase your overall VHDL proficiency. In this five-day course, you will gain valuable hands-on experience. Incoming students with little or no VHDL knowledge will finish this course empowered with the ability to write efficient hardware designs and perform high-level HDL simulations.

#### Lab Required- CAD Lab

#### Software Tools

- Xilinx ISE™ 9.2i
- ORCAD
- Mentor Graphics Modelsim Simulator

**Coordinators-** Ms. Deepali Garg, Ms. Sangeeta Patel and Ms. Malti Gautam

**Max Student Capacity-** 20 Students

**Applicable -** 3<sup>rd</sup> yr. Students

**Duration-** 30 hrs.

#### Who Should Attend?

Engineers who want to use VHDL effectively for modeling, design, and synthesis of digital designs

#### Prerequisites

Basic digital design knowledge

## Skills Gained

*After completing this training, you will know how to:*

- Implement the VHDL portion of coding for synthesis
- Identify the differences between behavioral and structural coding styles
- Distinguish coding for synthesis versus coding for simulation
- Use scalar and composite data types to represent information
- Use concurrent and sequential control structure to regulate information flow
- Implement common VHDL constructs (Finite State Machines [FSMs], RAM/ROM data structures)
- Simulate a basic VHDL design and see the RTL.
- Burn the VHDL code in the FPGA board.
- Write a VHDL test bench and identify simulation-only constructs

**XILINX Workshop Schedule**

<b>Date</b>	<b>Time</b>	<b>Topics</b>	<b>Description</b>
Day-1	9.30am -12.30pm	Introduction	<ul style="list-style-type: none"> <li>• ORCAD</li> </ul>
Day-2	9.30am -12.30pm	Circuit Designing	<ul style="list-style-type: none"> <li>• Combinational &amp; sequential Circuits</li> </ul>
Day-3	9.30am -12.30pm	Transient & Time Domain Analysis	<ul style="list-style-type: none"> <li>• Combinational &amp; sequential Circuits</li> </ul>
Day-4	9.30am -12.30pm	Introduction	<ul style="list-style-type: none"> <li>• What is VHDL</li> <li>• Using the Tools</li> <li>• Demo: Multiplexer</li> </ul>
Day-5	9.30am -12.30pm	Concurrent statement	<ul style="list-style-type: none"> <li>• Entity &amp; architecture</li> <li>• Using Concurrent Statements</li> <li>• Processes and Variables</li> </ul>
Day-5	9.30am -12.30pm	Simulation & FSM	<ul style="list-style-type: none"> <li>• ISim Simulation Tool Basics</li> <li>• Simulating a Simple Design</li> <li>• Creating Memory</li> <li>• Building a Dual-Port Memory</li> <li>• Finite State Machines</li> <li>• Building a Moore Finite State Machine</li> </ul>
Day-6	9.30am -12.30pm	FPGA implementation	<ul style="list-style-type: none"> <li>• Targeting Xilinx FPGAs</li> <li>• Xilinx Tool Flow</li> </ul>
Day-7	9.30am -12.30pm	Loops, packages & libraries	<ul style="list-style-type: none"> <li>• Loops and Conditional Elaboration</li> <li>• Attributes</li> <li>• Functions and Procedures</li> <li>• Packages and Libraries</li> </ul>
Day-8	9.30am -12.30pm	Test bench	<ul style="list-style-type: none"> <li>• Building Your Own Package</li> <li>• Interacting with the Simulation</li> <li>• Building a Meaningful Test bench</li> </ul>
Day- 9	9.30am -12.30pm	Mini Project	<ul style="list-style-type: none"> <li>• Choosing a mini project</li> <li>• Understanding the problem</li> </ul>
Day- 10	9.30am -12.30pm	Mini Project	<ul style="list-style-type: none"> <li>• Making of FSM</li> <li>• Start coding</li> </ul>
Day-11	9.30am -12.30pm	Mini Project	<ul style="list-style-type: none"> <li>• Finishing of coding</li> </ul>
Day-12	9.30am -12.30pm	Mini Project	<ul style="list-style-type: none"> <li>• Simulation</li> <li>• RTL generation</li> <li>• Burning on FPGA board</li> </ul>

**Coordinators-**  
**Ms. Deepali Garg**  
**Ms. Sangeeta Patel**  
**Ms. Malti Gautam**

**HOD (ECE)**  
**Dr. A. N. Mishra**